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EXAMINER	
PETRANEK, JACOB ANDREW	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 03/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/743,141	SODANI ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *04 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-25 are pending.

2. The office acknowledges the following papers:

Request for correct filing receipt filed on 6/3/2004

Oath and drawings filed on 5/5/2004.

Priority

3. No claim for priority has been made in this application.

Drawings

4. The Examiner contends that the drawings submitted on 5/4/2004 are acceptable for examination proceedings.

Specification

5. The disclosure is objected to because of the following informalities:

6. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. The Applicant's cooperation is requested in correcting any errors of which the Applicant may become aware.

7. Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

9. Claims 1-5, 8-9, 14-18, and 23-25 are rejected under 35 U.S.C. §102(e) as being anticipated by Kadambi et al. (U.S. 6,934,830).

10. As per claim 1:

Kadambi disclosed a processor comprising:

A register file (Kadambi: Figure 1 element 104, column 3 lines 6-12);

An execution unit (Kadambi: Figure 1 element 106, column 2 lines 66-67); and

A register file cache coupled to the register file and to the execution unit (Kadambi: Figure 1 element 102, column 3 lines 13-33)(A register file cache is a storage unit that stores instruction operands. The register pane is a storage unit smaller than the register file that stores instruction operands).

11. As per claim 2:

Kadambi disclosed the processor of claim 1, wherein the register file cache comprises a write-back portion to receive a result of an instruction executed by the execution unit (Kadambi: Figure 3 element 318, column 4 lines 24-35)(The register

pane has the ability to receive instruction execution results.).

12. As per claim 3:

Kadambi disclosed processor of claim 1, wherein the register file cache comprises a fill portion to receive an operand read from the register file (Kadambi: Figure 3 element 308, column 4 lines 36-39)(The register pane has the ability to receive instruction operands from the register file.).

13. As per claim 4:

Kadambi disclosed an apparatus comprising:

A first data storage structure to hold instruction operands (Kadambi: Figure 1 element 102, column 3 lines 13-33)(The register pane is a data storage structure that holds instruction operands.);

A second data storage structure to hold instruction operands, coupled to the first data storage structure (Kadambi: Figure 1 element 104, column 3 lines 6-12)(The register file is a data storage structure that holds instruction operands.); and

A logic device coupled to the first data storage structure and to the second data storage structure, to execute instructions using operands read from either the first data structure (Kadambi: Figure 3 elements 308 and 314, column 4 lines 24-39)(Instructions are executed using operands from the register pane. Operands needed that aren't present in the register pane are forwarded from the register file to the register pane so that an instruction can reissue.).

14. As per claim 5:

Kadambi disclosed the apparatus of claim 4, further comprising:

A data-management mechanism to move data corresponding to an operand from the second data storage structure to the logic device when the data is not present in the first data storage structure (Kadambi: Figure 3 element 308, column 4 lines 36-39).

15. As per claim 8:

Kadambi disclosed the apparatus of claim 4, wherein the first data storage structure includes a write-back portion to which to write results of instructions executed by the logic device (Kadambi: Figure 3 element 318, column 4 lines 24-35)(The instruction results are written back into the register pane.).

16. As per claim 9:

Kadambi disclosed the apparatus of claim 5, wherein the first data storage structure includes a fill portion, and the data-management mechanism is to copy the data from the second data storage structure to the fill portion (Kadambi: Figure 3 element 308, column 4 lines 36-39)(The register file writes operands to the register pane if an instruction needs an operand not currently present in the register pane.).

17. As per claim 14:

Kadambi disclosed the apparatus of claim 4, wherein the first data storage structure includes shared tracks (Kadambi: Figure 1 element 102, column 3 lines 13-33)(The bus lines are shared to write and read operands to the register pane.).

18. As per claim 15:

Kadambi disclosed a method comprising:

Arranging a register file cache to communicate with an execution unit and a register file (Kadambi: Figure 1 elements 102, 104, and 106, column 2 lines 66-67 and

column 3 lines 6-33)(A register file cache is a storage unit that stores instruction operands. The register pane is a storage unit smaller than the register file that will store instruction operands);

Searching the register file cache for an instruction operand of an instruction to be executed by the execution unit (Kadambi: Figure 3 element 304, column 3 lines 64-67 continued to column 4 lines 1-3); and

If the operand is found in the register file cache, reading the operand from the register file cache (Kadambi: Figure 3 element 314, column 4 lines 24-35).

19. As per claim 16:

Kadambi disclosed the method of claim 15, further comprising:

If the operand is not found in the register file cache, reading the operand from the register file (Kadambi: Figure 3 element 308, column 4 lines 36-39)(The operand is read and copied to the register pane.).

20. As per claim 17:

Kadambi disclosed the method of claim 16, further comprising:

Copying the operand that is read from the register file to the register file cache (Kadambi: Figure 3 element 310, column 4 lines 36-39).

21. As per claim 18:

Kadambi disclosed the method of claim 16, further comprising:

Executing the instruction (Kadambi: Figure 3 element 316, column 4 lines 24-35); and

Writing a result of the instruction to the register file cache (Kadambi: Figure 3

element 318, column 4 lines 24-35).

22. As per claim 23:

Claim 23 essentially recites the same limitations of claim 1. Claim 23 additionally recites the following limitations:

A memory to hold instructions for execution (Kadambi: Figure 1 element 108, column 3 lines 2-5).

23. As per claim 24:

Claim 24 essentially recites the same limitations of claim 2. Therefore, claim 24 is rejected for the same reasons as claim 2.

24. As per claim 25:

Claim 25 essentially recites the same limitations of claim 3. Therefore, claim 25 is rejected for the same reasons as claim 3.

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claims 21 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kadambi et al. (U.S. 6,934,830).

27. As per claim 21:

Kadambi disclosed the method of claim 18.

Kadambi failed to teach allocating a register in the register file cache to which to write the instruction result, such that the result will be written to the register only when all outstanding reads of contents of the register have completed.

However, it would have been obvious to one of ordinary skill in the art at the time of the invention that an allocated register in the register pane can't be overwritten before all instructions have read the operand. Failing to do this will lead to the program not working correctly when an instruction gets the overwritten value of a register operand within the register pane instead of the original contents.

28. Claims 6-7, 10-12, 19-20, and 22 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kadambi et al. (U.S. 6,934,830), further in view of Choquette (U.S. 6,088,784)

29. As per claim 6:

Kadambi disclosed the apparatus of claim 5.

Kadambi failed to teach a write-back mechanism to move data from the first data storage structure to the second data storage structure.

However, Choquette disclosed a write-back mechanism to move data from the first data storage structure to the second data storage structure (Choquette: Figure 2 element 104, column 3 lines 56-64)(The global bypass unit has the ability to select an instruction result either staying in the bypass unit or being written back to the register file.).

The processor of Kadambi writes all execution results into both the register pane

and the register file. While this is a simple policy of keeping the two memories synchronized, it's a very wasteful process in terms of power consumption. The processor of Choquette eliminates most of these writes by determining which execution results should be stored within the global bypass structure and which results should be written back to the register file. This process results in many fewer writes to the register file because the results in the global bypass will likely be used many times before needing to be written back. The advantage of saving power consumption would have motivated one of ordinary skill in the art at the time of the invention to implement the register pane of Kadambi with the ability to selectively write back instruction results. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the register pane that can write back instruction results selectively for the advantage of reduced power consumption.

30. As per claim 7:

Kadambi and Choquette disclosed the apparatus of claim 6, wherein the write-back mechanism moves the data based on a frequency of access to the data (Kadambi: Figure 3 element 310, column 4 lines 40-49)(The replaced entries are chosen based on a LRU scheme. The combination of the global bypass and register pane functionality results in data being moved back based on a LRU scheme if the register pane is full of operands.).

31. As per claim 10:

Kadambi disclosed the apparatus of claim 4.

Choquette disclosed a write-back mechanism to move data from the first data

storage structure to the second data storage structure (Choquette: Figure 2 element 104, column 3 lines 56-64)(The global bypass unit has the ability to select an instruction result either staying in the bypass unit or being written back to the register file.).

The processor of Kadambi writes all execution results into both the register pane and the register file. While this is a simple policy of keeping the two memories synchronized, it's a very wasteful process in terms of power consumption. The processor of Choquette eliminates most of these writes by determining which execution results should be stored within the global bypass structure and which results should be written back to the register file. This process results in many fewer writes to the register file because the results in the global bypass will likely be used many times before needing to be written back. The advantage of saving power consumption would have motivated one of ordinary skill in the art at the time of the invention to implement the register pane of Kadambi with the ability to selectively write back instruction results. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the register pane that can write back instruction results selectively for the advantage of reduced power consumption.

Kadambi and Choquette failed to teach wherein the first data storage structure is more ported than is the second data storage structure.

However, it would have been obvious to one of ordinary skill in the art that the register file could have fewer ports than the combination of the register pane with the elements of the global bypass unit. One of ordinary skill in the art would see that the combination likely will lead to fewer writes being needed to the register file and fewer

reads should be inherent within the processor of Kadambi because a majority of the operand reads are done from the register pane to ensure better performance. The resulting fewer register writes and reads to/from the register file would lead to the ability to have fewer read and write ports on the register file compared to the register pane. One of ordinary skill in the art would have been motivated at the time of the invention to have fewer ports on the register file in order to reduce power consumption and cost from the register file. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the register file with fewer ports than the register pane because of the advantages from reduced power consumption and costs of the register file.

32. As per claim 11:

Kadambi disclosed the apparatus of claim 4.

Choquette disclosed a write-back mechanism to move data from the first data storage structure to the second data storage structure (Choquette: Figure 2 element 104, column 3 lines 56-64)(The global bypass unit has the ability to select an instruction result either staying in the bypass unit or being written back to the register file.).

The processor of Kadambi writes all execution results into both the register pane and the register file. While this is a simple policy of keeping the two memories synchronized, it's a very wasteful process in terms of power consumption. The processor of Choquette eliminates most of these writes by determining which execution results should be stored within the global bypass structure and which results should be written back to the register file. This process results in many fewer writes to the register

file because the results in the global bypass will likely be used many times before needing to be written back. The advantage of saving power consumption would have motivated one of ordinary skill in the art at the time of the invention to implement the register pane of Kadambi with the ability to selectively write back instruction results. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the register pane that can write back instruction results selectively for the advantage of reduced power consumption.

Kadambi and Choquette failed to teach an allocation mechanism to allocate a register in the first data structure to which to write an instruction result, wherein the allocate mechanism is to allocate the register such that the result will be written to the register only when all outstanding reads of contents of the register have completed.

However, it would have been obvious to one of ordinary skill in the art at the time of the invention that an allocated register in the register pane can't be overwritten before all instructions have read the operand. Failing to do this will lead to the program not working correctly when an instruction gets the overwritten value of a register operand within the register pane instead of the original contents.

33. As per claim 12:

Kadambi and Choquette disclosed the apparatus of claim 11, further comprising a write-back mechanism to move data from the first data storage structure to the second data storage structure, wherein the write-back mechanism is to cooperate with the allocation mechanism such that previous contents of the register will have been moved to the second data structure before the contents are overwritten by the result

(Choquette: Figure 2 element 104, column 3 lines 56-64)(It's inherent that the contents of the combined register pane and global bypass would be moved back to the register file before being overwritten with new contents from one of the execution units. If this did not happen, then the program would eventually fail from having execution contents lost before they were written back to the register file.).

34. As per claim 19:

Kadambi disclosed the method of claim 15.

Kadambi failed to teach periodically writing data from the register file cache to the register file.

However, Choquette disclosed periodically writing data from the register file cache to the register file (Choquette: Figure 2 element 104, column 3 lines 56-64)(A register file cache is a storage unit that stores instruction operands. The combined global bypass unit and register pane stores instruction operands and has the ability to either write instruction results back to the register file or store the results in the global bypass unit.).

The processor of Kadambi writes all execution results into both the register pane and the register file. While this is a simple policy of keeping the two memories synchronized, it's a very wasteful process in terms of power consumption. The processor of Choquette eliminates most of these writes by determining which execution results should be stored within the global bypass structure and which results should be written back to the register file. This process results in many fewer writes to the register file because the results in the global bypass will likely be used many times before

needing to be written back. The advantage of saving power consumption would have motivated one of ordinary skill in the art at the time of the invention to implement the register pane of Kadambi with the ability to selectively write back instruction results. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the register pane that can write back instruction results selectively for the advantage of reduced power consumption.

35. As per claim 20:

Kadambi and Choquette disclosed the method of claim 19, wherein the data are written based on a least-recently-used policy (Kadambi: Figure 3 element 310, column 4 lines 40-49)(The combination of the register pane and the global bypass unit replaces entries based on a LRU scheme.).

36. As per claim 22:

Kadambi disclosed the method of claim 18, further comprising:

Allocating a register in the register file cache to which to write the instruction result (Kadambi: Figure 3 element 318, column 4 lines 24-35);

Kadambi failed to teach periodically writing data from the register file cache to the register file and timing the allocating and the periodic writing such that previous contents of the register will have been moved to the register file before the contents are overwritten by the result.

However, Choquette disclosed periodically writing data from the register file cache to the register file (Choquette: Figure 2 element 104, column 3 lines 56-64)(A register file cache is a storage unit that stores instruction operands. The combined

global bypass unit and register pane stores instruction operands and has the ability to either write instruction results back to the register file or store the results in the global bypass unit.); and

Timing the allocating and the periodic writing such that previous contents of the register will have been moved to the register file before the contents are overwritten by the result (Choquette: Figure 2 element 104, column 3 lines 56-64)(It's inherent that the contents of the combined register pane and global bypass would be moved back to the register file before being overwritten with new contents from one of the execution units. If this did not happen, then the program would eventually fail from having execution contents lost before they were written back to the register file.).

The processor of Kadambi writes all execution results into both the register pane and the register file. While this is a simple policy of keeping the two memories synchronized, it's a very wasteful process in terms of power consumption. The processor of Choquette eliminates most of these writes by determining which execution results should be stored within the global bypass structure and which results should be written back to the register file. This process results in many fewer writes to the register file because the results in the global bypass will likely be used many times before needing to be written back. The advantage of saving power consumption would have motivated one of ordinary skill in the art at the time of the invention to implement the register pane of Kadambi with the ability to selectively write back instruction results. Thus, it would have been obvious to one of ordinary skill in the art at the time of the

invention to implement the register pane that can write back instruction results selectively for the advantage of reduced power consumption.

37. Claim 13 is rejected under 35 U.S.C. §103(a) as being unpatentable over Kadambi et al. (U.S. 6,934,830), further in view of Zaitzeva et al. (U.S. 5,781,924)

38. As per claim 13:

Kadambi disclosed the apparatus of claim 4.

Kadambi failed to teach wherein the first data storage structure comprises a first section and a second section, each of the first and second sections being divided into a plurality of subsections, wherein a subsection of the first section and a subsection of the second section have an exclusive set of write paths thereto.

However, Zaitzeva disclosed the first data storage structure comprises a first section and a second section, each of the first and second sections being divided into a plurality of subsections, wherein a subsection of the first section and a subsection of the second section have an exclusive set of write paths thereto (Zaitzeva: Figure 1 element 110, column 2 lines 8-65)(Each port writes to a separate section that contains subsections.).

The processor of Kadambi contains a register pane that is a cache smaller in size of the register file (Kadambi: Column 3 lines 13-33). The register pane can be arranged in a set-associative manner (Kadambi: Column 4 lines 4-23). Kadambi failed to teach how the actual implementation of a set-associative cache works. However, Zaitzeva disclosed a set-associative cache that works on multiple ports. Thus, it would

have been obvious to one of ordinary skill in the art at the time of the invention to search to find out a set-associative cache functionally works, such as how the cache is implemented in Zaitzeva.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nguyen et al. (U.S. 6,986,024), taught two data structures that hold instruction operands and the execution units being able to select with unit an operand will be used from.

Sutherland (U.S. 5,838,939), taught a processor system that uses a register file and a register file cache to increase performance.

Cheong et al. (U.S. 5,805,906), taught two data structures that hold instruction operands with one structure writing back results to the other structure.

Sami et al. (U.S. 6,889,317), taught a processor that can inhibit register writes and solely write operands to an instruction bypass buffer.

Stravers (U.S. 6,862,677), taught a system that eliminates certain types of writes back to registers from a buffer.

Cherabuddi (U.S. 6,263,416), taught many different types of data storage structures that can hold instruction operands.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner
Art Unit 2183

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100